Notice of Allowability	Application No.	Applicant(s)	
	10/619,463	FUKUOKA ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *09/29/06*.

2. ☒ The allowed claim(s) is/are *15-23*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 7/16/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Allowable Subject Matter

1. Claims 15-23 are allowed.

2. The following is an examiner's statement of reasons for allowance: the present invention features:

Closed related Prior Art:

US 5,883,855 (Fujita et al) teaches a semiconductor memory device having an input circuit for inputting reference clocks, an input buffer circuit for latching external input signals in synchronization with the reference clocks, and an output buffer circuit for outputting a stored data to an outside in synchronization with the reference clocks, the input buffer circuit and the output buffer circuit are caused to operate at respectively different edges of the reference clocks for processing one and the same stored data.

US 5,371,880 (Bhattacharya) teaches optimizing transmission of signals or events, a chipset permitting to choose whether the originating events are to be generated synchronously or asynchronously with the clock signal, where the number of destination clock cycles to delay before generating the desired destination bus event is responsive to the relative frequencies of the clock signals.

JP 04178580A (Akiyama) teaches Self-diagnostic semiconductor memory checking system having test detector connected for setting range of addresses in memory where a range of memory addresses to be tested are loaded into the

test finish detector, a separate clock generator provides enabling timing clock pulses to the address generator, data generator and memory in response to a test start signal.

However, none of the prior art of record teaches or renders obvious the features recited in the claims, specifically:

an address conversion circuit comprising a gated logic circuit, a clock enable generating circuit, a tag memory and a data memory,

wherein the clock enable generating circuit invalidating a clock enable signal when a first logical page address requested as a preceding access is the same as a second logical page address requested as a present access and a first intra-page address requested as the present access is not within the boundary addresses between intra-page addresses, and

the gated logic circuit cutting off the clock to the tag memory and the data memory when the clock enable signal is valid.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon-Fri (8:00A to 4:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

November 9, 2006